CLAIM AMENDMENTS

1.-20. (Cancelled)

21. (New) A method comprising:

receiving an indication of bits of incoming data from a first serial bus;

buffering the bits to accommodate a difference between a first rate of the incoming data and a second rate of outgoing data;

during the buffering, detecting whether at least some of the bits indicate a synchronization field;

detecting valid logic levels on the first serial bus; and

selectively enabling a transmitter to communicate the incoming data to a second serial bus based on the detection of whether at least some of the bits indicate the synchronization field and the detection of valid logic levels on the first serial bus.

22. (New) The method of claim 21, further comprising:

buffering the synchronization field; and

communicating the buffered synchronization field to the second serial bus.

23. (New) The method of claim 21, wherein the buffering comprises:

passing the bits through a delay line.

24. (New) The method of claim 21, wherein the detecting comprises:

comparing at least some of the bits to an indication of a predetermined bit pattern.

25. (New) A system comprising:

a first serial bus;

a second serial bus; and

a repeater coupled to the first and second serial busses to receive an indication of bits of incoming data from the first serial bus, concurrently buffer the bits to accommodate a difference between a first rate of the incoming data and a second rate of outgoing data and, detect whether at least some of the bits indicate a synchronization field, detect valid logic levels on the first serial bus, and selectively enable transmission to the second serial bus based on the detection of the synchronization field and the detection of valid logic levels on the first serial bus.

26. (New) The system of claim 25, wherein the repeater comprises:

a receiver to receive an indication of bits of the incoming data from the first serial bus; and

a transmitter to communicate the bits to a second serial bus to form the outgoing data.

27. (New) The system of claim 26, further comprising:

a synchronization circuit to detect the synchronization field and selectively enable the transmitter in response to the detection.

28. (New) The synchronization circuit of claim 25, wherein the synchronization detection circuit comprises:

a comparator to compare at least some of the bits to an indication of a predetermined bit pattern to perform the detection.